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Design of Efficient adder Circuits in Sub Threshold Region

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Abstract: Sub threshold (leakage or cut-off) currents are a necessary in traditional VLSI design methodologies. Ultra-low power applications such as micro-sensor networks, pacemakers, and many portable devices require extreme energy constraints for longer battery life. Increasing the battery life can provide a competitive advantage in the marketplace. Traditionally, reducing the power supply voltage is regarded as the most effective means of reducing power consumption. Therefore, digital circuits operating in the sub threshold region offer a promising solution for emerging portable applications that require tremendously low energy consumption. The proposed work is to compare the performance of various CMOS circuits such as inverter, Half adder, Full adder between conventional conduction and sub threshold conduction in terms of power and delay. As a result the circuits under sub threshold conduction is efficient than conventional because power of sub threshold circuit is less than conventional circuit. The circuits are design using tanner tool.

Keywords: Sub threshold conduction, combinational circuits, low power.

I INTRODUCTION

In energy-consuming systems, low power design is essential for efficient battery life time. Lowering supply voltage (V_{dd}) leads to decrease in energy dissipation increase in delay. The required performance can be obtained by reducing the threshold voltage (V_{th}) of the device that achieves low power. The most important parameter controlling power consumption is the supply voltage. By scaling the supply voltage below the value of threshold voltage, the circuit can become Sub threshold circuit design, where load capacitances are charged/discharged by sub threshold leakage currents [8]. So sub threshold circuits have its applications on ultra-low power dissipation, with average circuit performance.
The power consumption in CMOS is given by

$$P_g = f_d C_L V_{DD}^2$$

V_{DD} is the supply voltage, C_L is the switched capacitance of the circuit, $P_g$is the power consumption of one gate, F_d is the average operating frequency of that gate.

II SUBTHRESHOLD CONDUCTION

Sub threshold conduction is the current between the source and drain of aMOSFET when the transistor is in sub threshold region, for gate-to-source voltages below the threshold voltage. Sub threshold conduction is generally viewed as a parasitic leakage. Sub threshold logic operates with the power supply V_{dd} less than the transistors threshold voltage Vt [1][5]. In micro power analog circuits, weak inversion is an efficient operating region, and sub threshold is a useful transistor mode around which circuit functions are designed. The sub threshold conduction of transistors are small in the off state, when gate voltage is below threshold value. Sub threshold conduction is the major component of leakage. Some other leakage components may depends on the device design as gate-oxide leakage and junction leakage. By getting solutions for such leakages gives the better circuit design.
The conventional conduction leads to high leakage power. There are various methods available to reduce such leakage power which may result in reduction of performance in terms in speed and delay. So in order to overcome such disadvantages and trade-offs, Sub threshold conduction arrives, in which the circuit start conduction within the sub threshold region before input voltage reaches the threshold voltage.
The relationship between W/L and source drain current is equally simple [9]. As the channel width increases, more carriers are available to conduct current. As channel length increases, however the drain to source voltage dimensions in effect. V_{ds} is the potential energy available to push carriers from drain to source, as the distance From drain to source, as the distance from D and S increases, it takes longer to push carriers across the transistor for a fixed V_{ds}, reducing current flow.

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TRANSISTOR SIZING

The devices with equal sized transistor width can lead to low power circuit without affecting the performance.
The major solution is just by increasing the transistor size, the power can be reduced [3][6]. This results in reduced resistance and time constant. But it includes a disadvantage that it results in large parasitic capacitor. It also affects the propagation delay.

III BEHAVIOUR OF NMOS WITH DIFFERENT REGIONS

The behavior of NMOS with different regions can be classified into the following three cases:

A.CUT-OFF REGION

In this region $V_{gs}<V_t$, The source and drain have free electrons. The body has free holes but no free electrons.

$$I_{ds}=0$$

The junction between the body and the source of drain is reverse-biased. So no current will flow. This mode of operation is called cutoff.

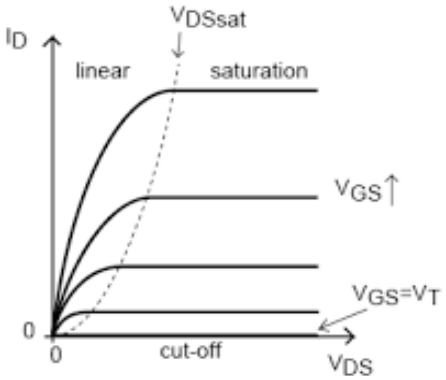

Fig 1. IV Characteristics of MOSFET

B. LINEAR REGION

In this region, $V_{gs}>V_t$. Now an inversion regionof electrons called the channel connects the source and drain. This creates a conductive path between source and drain. The number of carriers and the conductivity increases with the gate voltages. The potential difference between drain and source is $V_{ds}=V_{gs}-V_{gd.}$ If $V_{ds}=0$, there is no electric field tending to push current from drain and source.

$$I_{ds} = \beta[(V_{gs}-V_t)V_{ds}-V_{ds}^2/2]$$

When a small positive potential V_{ds} is applied to drain, current I_{ds} flows through the channel from drain and source. This mode of operation is called linear or resistive or nonsaturated or unsaturated mode. In this current increases with both the drain voltage and gate voltage.

C. SATURATION REGION

In this region, if V_{ds}becomes sufficiently large than $V_{gd}<V_t$, the channel is no longer inverted near the drain and become pinched off. But conduction is brought about by the drift of electrons under the positive drain voltage. As electrons reach the end of the channel, they are injected into the depletion region near the drain and accelerated toward the drain.

$$I_{ds} = \beta/2(V_{gs}-Vt)^2$$

For high V_{DS}, carriers experience higher lateral electric fields. Carrier velocity increases with increasing lateral electric fields. However, once the critical lateral electric field is reached, the velocity of the carriers does not increase. This is caused by an increased rate of collision and carrier scattering. The current does not increase at the expected rate.

IV PROPOSED WORK

A. Simulation of inverter:

In conventional inverter circuit that it start conducts on after reaches it threshold value.

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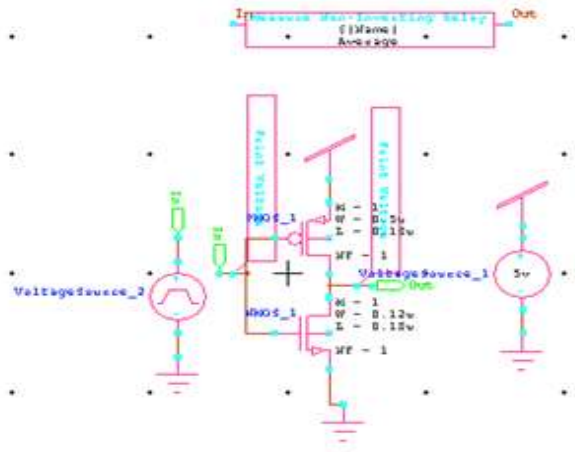

Fig 2.schematic of conventional inverter

In this sub threshold inverter that starts conduction before the input reaches the threshold value. Inverter is the Complementary circuit where output will bethe complement of input.

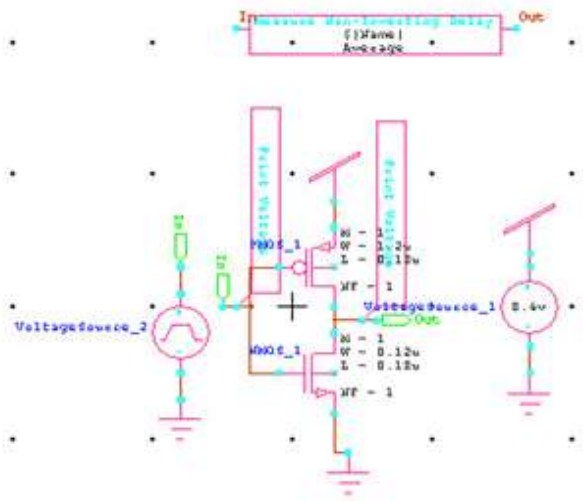

Fig 3.schematic of sub threshold inverter

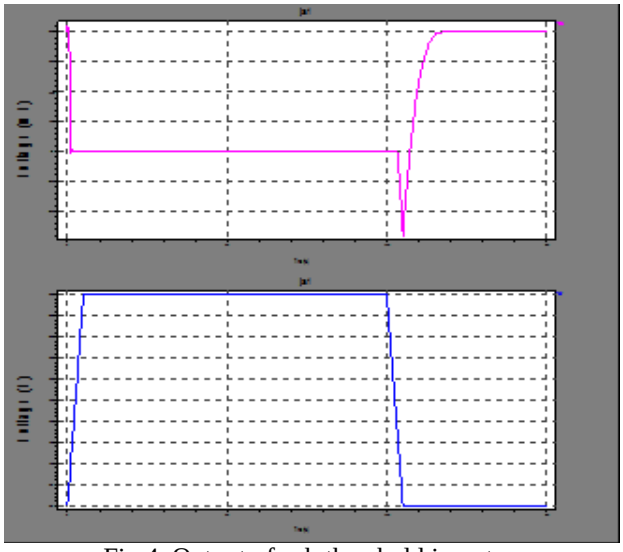

Fig 4. Output of sub threshold inverter

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Fig 4 shows the output waveform of sub threshold inverter. When A=1, then output y will be complement of a as Y=0.

B. Simulation of half adder

The sub threshold half adder that starts conduction before the input reaches the threshold value. It consists of two inputs and two outputs are sum and carry.

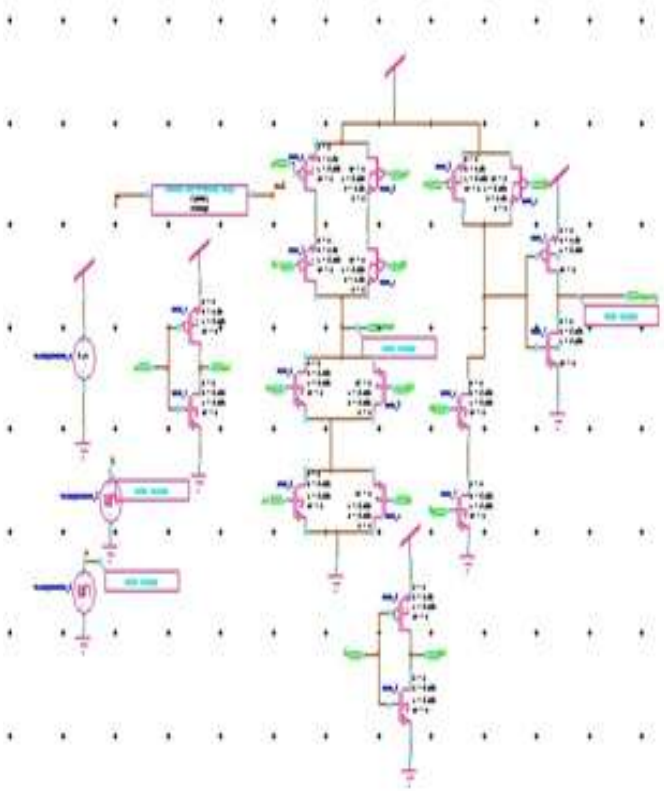

Fig 5. schematic of sub threshold half adder

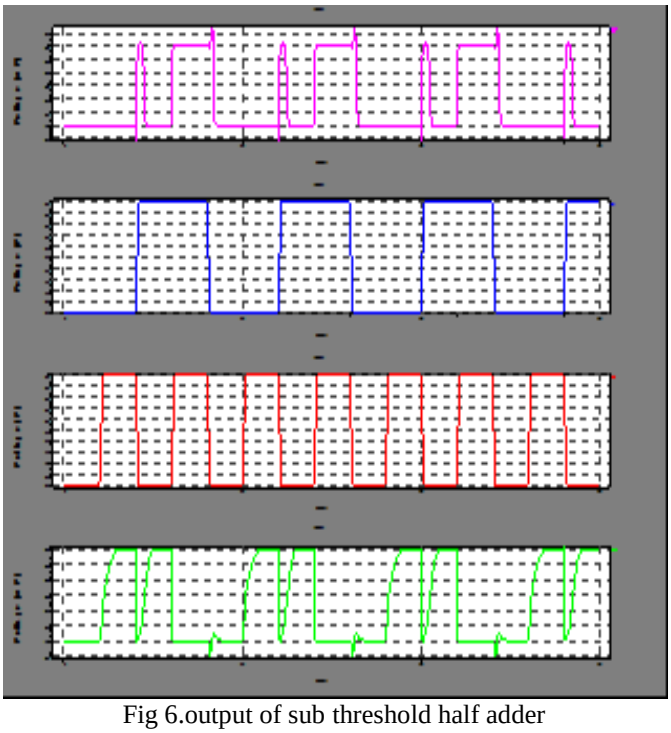

Fig 6.output of sub threshold half adder

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Fig 6Shows the output waveform of sub threshold half adder. When A=1 and B=0, The sum value is 1 and carry value is 0.

C. Simulation of full adder

The sub threshold full adder that starts conduction before the input reaches the threshold value. It consists of three inputs and two outputs are sum and carry.

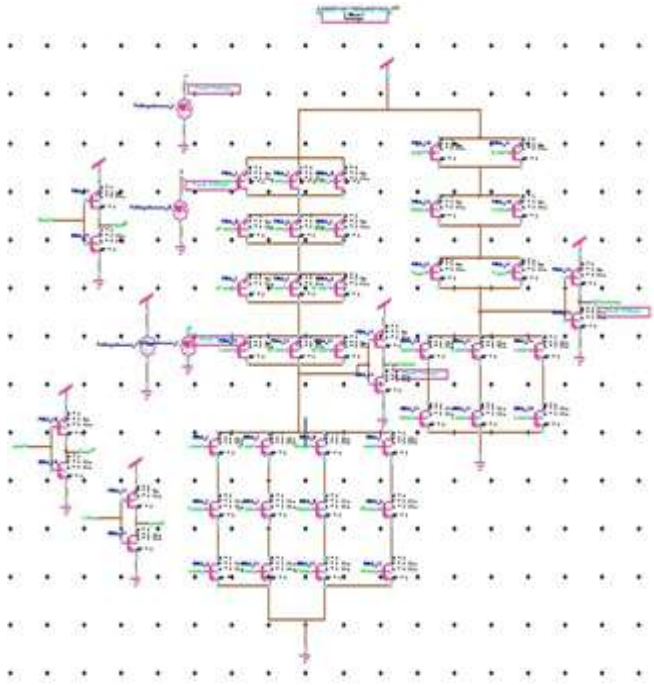

Fig 7.schematic of sub threshold full adder

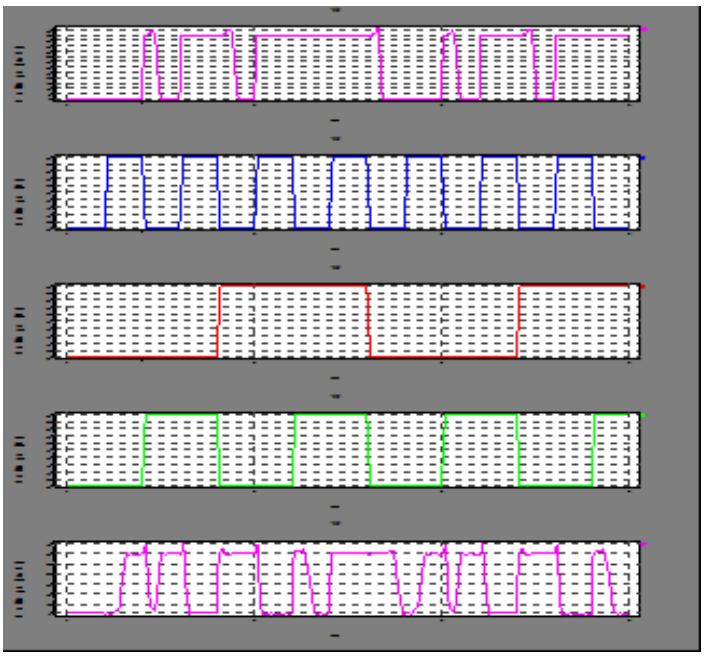

Fig8. Output of sub threshold full adder

Fig 8 shows the output waveform of sub threshold full adder When A=1 and B=0, Cin=0, The sum value is 1 and carry value is 0.

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Table I. Comparison table of conventional and sub threshold gates

GATES		CONVENTIONAL	SUB THRESHOLD
Inverter	Power	20.46KW	38.902mW
	Delay	0.00154ms	37.59ms
Half adder	Power	31.8KW	301053Mw
	Delay	8.33ms	23.512ms
Full adder	Power	34.16Kw	1.706mw
	Delay	15.22ms	50.907ms

Table I shows the comparison of calculated power and delay for both conventional and sub threshold circuits. The power can be reduced due to the sub threshold conduction.

V. CONCLUSION

The width of PMOS is varied to be operated in sub threshold region. Some circuits such as CMOS Inverters, Half adder and Full adder in sub threshold region was simulated the performance analyses in terms of Power and Delay are compared between conventional and sub threshold conduction. The comparison shows that the power consumption is less and delay is more in sub threshold when compared to Conventional (Strong Inversion Region).

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